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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,751	07/28/2003	Kun-Hong Chen	LEE0015-US	4408
24504	7590	06/01/2005	EXAMINER	
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 100 GALLERIA PARKWAY, NW STE 1750 ATLANTA, GA 30339-5948			NGUYEN, KHIEM D	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/627,751

Applicant(s)

CHEN, KUN-HONG

Examiner

Khiem D. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 8,9 and 11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 8,9 and 11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

New Grounds of Rejection

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 8, 9 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Dai et al. (U.S. Patent 6,677,189).

In re claim 8, **Dai** discloses a method of forming a lightly doped drain in a thin film transistor, comprising:

providing a glass substrate 30 and a polysilicon structure 32 on the glass substrate 30 (col. 2, lines 53-57 and FIG. 2A);

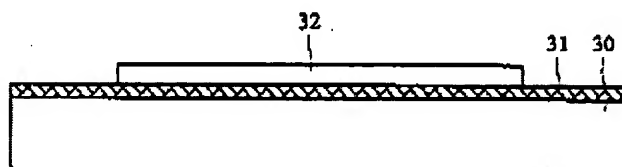


FIG. 2A

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depositing an insulating layer 34 on the polysilicon structure 32 and the glass substrate 30; depositing a metal layer 38 on the insulating layer 34 (col. 2, lines 57-60 and FIG. 2B);

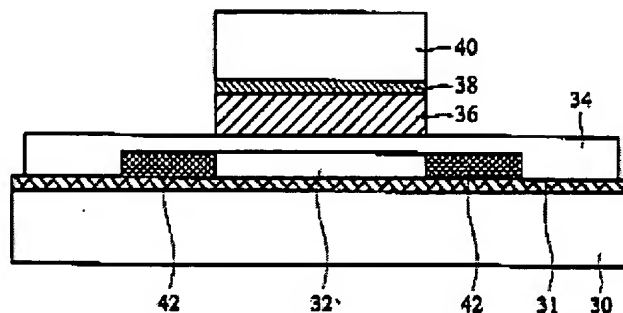


FIG. 2B

forming a photo resist layer 40, having a transferred, pattern on the metal layer 38 (col. 2, lines 60-64 and FIG. 2B);

dry etching a portion of the metal layer 38 to expose a portion of the insulating layer 34, using the photo resist layer 40 as a first mask (col. 2, line 64 to col. 3, line 1);

implanting multiple (M) first ions through the insulating layer 34 into the polysilicon structure 32, using the photo resist layer 40 and the metal layer 38 as a second mask (col. 3, lines 2-8 and FIG. 2B);

isotropic etching a portion of the metal layer 38 such that undercut 39 of the metal layer under the photo resist layer 40 is observed (col. 3, line 9-12 and FIG. 2C);

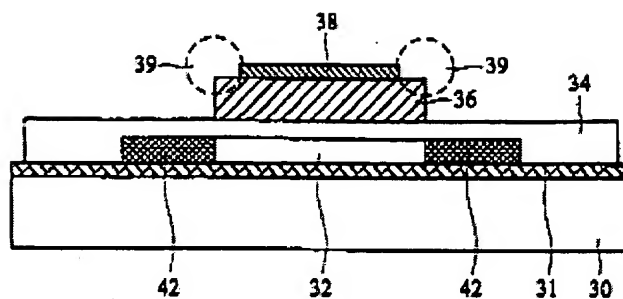


FIG. 2C

removing the photo resist layer 40 (col. 3, lines 12-13 and FIG. 2D); and

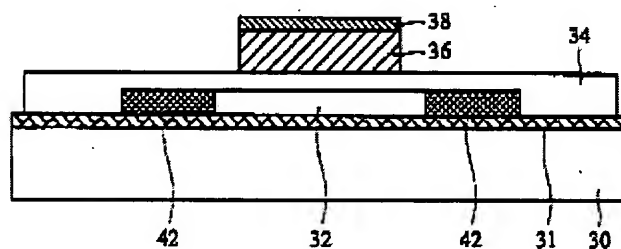


FIG. 2D

implanting multiple (M) second ions into the polysilicon structure 32 to form the lightly doped drain 44, using the undercut metal layer 38 as a third mask (col. 3, lines 13-41 and FIG. 2E).

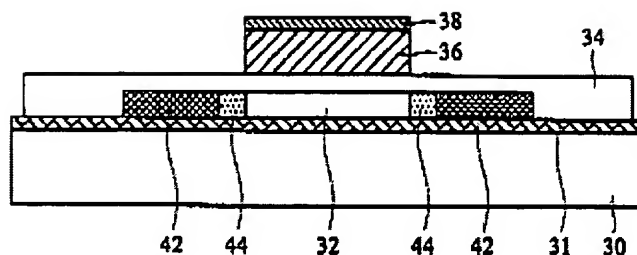


FIG. 2E

In re claim 9, Dai discloses that the step of isotropic etching comprises wet etching a portion of the metal layer (col. 3, lines 9-12).

In re claim 11, Dai discloses a method of forming a lightly doped drain, the lightly doped drain is formed in a thin film transistor, comprising:

providing a glass substrate 30 and a polysilicon structure 32 on the glass substrate 30 (col. 2, lines 53-57 and FIG. 2A);

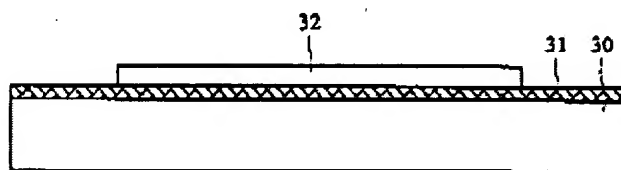


FIG. 2A

depositing an insulating layer 34 on the polysilicon structure 32 and the glass substrate 30; depositing a metal layer 38 on the insulating layer 34 (col. 2, lines 57-60 and FIG. 2B);

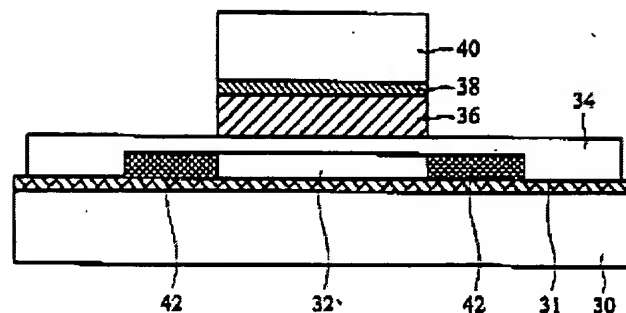


FIG. 2B

forming a photo resist layer 40, having a transferred, pattern on the metal layer 38 (col. 2, lines 60-64 and FIG. 2B);

dry etching a portion of the metal layer 38 to expose a portion of the insulating layer 34, using the photo resist layer 40 as a first mask (col. 2, line 64 to col. 3, line 1);

implanting multiple (M) first ions through the insulating layer 34 into the polysilicon structure 32, using the photo resist layer 40 and the metal layer 38 as a second mask (col. 3, lines 2-8 and FIG. 2B);

isotropic etching a portion of the metal layer 38 such that undercut 39 of the metal layer under the photo resist layer 40 is observed, the step of isotropic etching including a step of wet etching (col. 3, lines 9-12 and FIG. 2C);

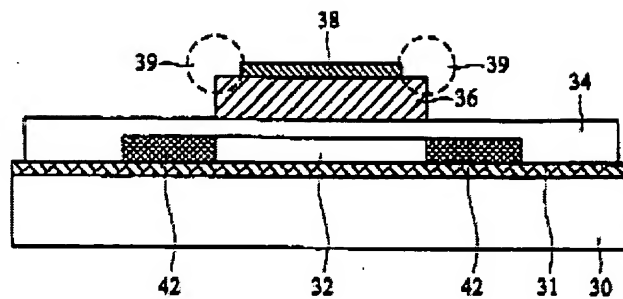


FIG. 2C

removing the photo resist layer 40 (col. 3, lines 12-13 and FIG. 2D); and

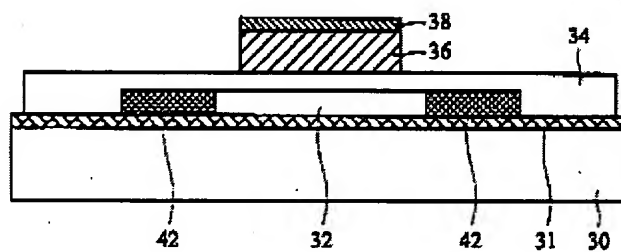


FIG. 2D

implanting multiple (M) second ions into the polysilicon structure 32 to form the lightly doped drain 44, using the undercut metal layer as a third mask (col. 3, lines 13-14 and FIG. 2E).

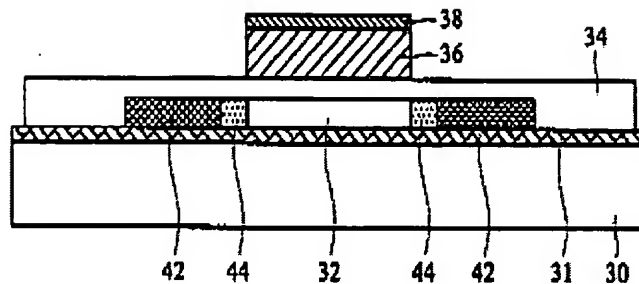


FIG. 2E

Response to Applicant's Amendment and Arguments

Applicant's arguments with respect to claims 8-9 and 11 have been considered but are moot in view of the new ground(s) of rejection.

Applicant contends that the You reference neither teaches nor suggest the method of implanting ions through the insulating layer.

In response to Applicant's contention that the You reference neither teaches nor suggest the method of implanting ions through the insulating layer. Since Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action, Examiner respectfully submits that Applicant's argument is moot in view of the newly discovered reference to Dai et al. (U.S. Patent 6,677,189), applied under 35 U.S.C. 102(e) rejection presented in this Office Action. Applicant is directed to page 3, 2nd paragraph of this Office Action where Dai discloses implanting multiple (M) first ions through the insulating layer 34 into the polysilicon structure 32, using the photo resist layer 40 and the metal layer 38 as a second mask (col. 3, lines 2-8 and FIG. 2B, Dai et al.).

For this reason, Examiner holds the rejection proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
May 27th, 2005



W. DAVID COLEMAN
PRIMARY EXAMINER